

UNITED STATES PATENT APPLICATION FOR

CURRENT LIMITING VOLTAGE REGULATION CIRCUIT

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CURRENT LIMITING VOLTAGE REGULATION CIRCUIT TECHNICAL FIELD

The present invention generally pertains to the field of electronic circuits. More particularly, embodiments of the present invention are
5 related to limiting output current in a voltage regulation circuit.

BACKGROUND ART

Many electronic circuits have a need for limiting current. Voltage regulators and battery chargers are two examples of circuits needing
10 current limit protection, although many other circuits also need current limit protection. Voltage regulators provide a substantially constant voltage over a range of load impedances. However, if the load impedance is relatively small, the voltage regulator must output a very large current to maintain the output voltage. Such a large current can lead to overheating
15 and damage or destruction of the output transistor, as well as nearby components. Frequently it is impractical to provide a heat sink for the voltage regulator due to, for example, space or economic constraints and packaging constraints.

20 Thus, a need exists for a current limiting circuit for an electronic circuit. A still further need exists for a current limiting circuit that is compatible with and can be fabricated economically with existing semiconductor fabrication techniques.

SUMMARY

The present invention provides current limiting in a voltage regulation circuit. Embodiments of the present invention provide current limit protection circuits that are compatible with and can be fabricated
5 economically with existing semiconductor fabrication techniques.

A current limiting voltage regulation circuit is disclosed. In one embodiment in accordance with the present invention, the circuit comprises a device coupled to an output node of the current limiting circuit.
10 The device is responsive to magnitude of a signal at the output node. Moreover, the device has a first mode and a second mode depending on the magnitude of the signal. The current limiting circuit also has a regulation component coupled to the device and that regulates a voltage at the output node when the device is in the first mode. The current limiting circuit also
15 has an element coupled to the device that has a current that limits current at the output node when the device is in the second mode.

In one embodiment, the current limiting voltage regulation circuit comprises an output transistor, an error amplifier, and first and second
20 transistors. The error amplifier has one input that receives a reference voltage and another input that is coupled to the output transistor to receive a scaled version of a regulated output voltage. The first transistor is coupled between a control terminal of the output transistor and an output of the

error amplifier. The first transistor is responsive to the magnitude of a signal at the output transistor, wherein the first transistor has a first mode and a second mode depending on the magnitude of the signal. The second transistor is coupled to the first transistor and the output transistor,
5 wherein a current through the second transistor is mirrored in the output transistor if the first transistor is in the second mode. Moreover, the error amplifier regulates the regulated voltage if the first transistor is in the first mode.

10 Another embodiment of the present invention is a method of limiting current and regulating voltage. The method comprises sensing a signal at an output node. If the signal is below a pre-determined threshold, a voltage at the output node is regulated. If the signal is above the pre-determined threshold, a current at the output node is limited without regulating the
15 voltage at the output node.

These and other advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are
20 illustrated in the various drawing figures.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the
5 invention:

Figure 1 is a schematic of a circuit for limiting current and regulating voltage, according to an embodiment of the present invention.

10 Figure 2 is a schematic of a circuit for limiting current and regulating voltage using a cascode transistor, according to an embodiment of the present invention.

Figure 3 is a flowchart illustrating steps of a process of limiting
15 current in a voltage regulation circuit, according to embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

Figure 1 is a schematic of a circuit for limiting current and regulating voltage, according to an embodiment of the present invention. The circuit 100 of Figure 1 includes two operating modes. One of the modes may be termed a “voltage regulation” operating mode in which the error amplifier 110 regulates the output voltage V_{out} . The other operating mode may be termed a “current-limiting” mode in which an output current is limited. For example, the drain to source current of output transistor M3 is

limited. In the current limiting mode, the error amplifier 110 may not regulate the output voltage V_{out} . Rather, the circuit 100 operates in a current regulation mode, in which a current (e.g., I_{M1}) is used to regulate and limit the output transistor current I_{M3} . The current limiting mode may
5 be used as protection if, for example, the load impedance Z_{load} is so low that the output transistor current I_{M3} would be at an unsafe level without the current protection. Thus, the circuit 100 provides protection against short circuits, as well as low load impedance situations. The actual current that results in an unsafe power level could be virtually any level, depending on
10 input voltage (V_{dd}), output voltage (V_{out}), construction of output transistor $M3$, and environment.

The circuit 100 comprises an error amplifier 110 that regulates the output voltage V_{out} , during a voltage regulation operating mode. The error
15 amplifier 110 has a reference voltage V_{ref} as an input to its negative input. Its positive input is coupled between output resistors $R1$ and $R2$. The output of the error amplifier 110 is coupled to the gate $G3$ of the output transistor $M3$ via transistor $M2$. Thus, the voltage regulation loop includes the transistor $M2$, which will be discussed in more detail below. Output
20 resistor $R2$ is coupled to ground and output resistor $R1$ is coupled to the output transistor $M3$, such that the output voltage V_{out} may be set relative to the reference voltage V_{ref} , based on the sizes of output resistors $R1$ and $R2$.

The transistor M2 may be referred to throughout this description as a range-limited buffer. The range-limited buffer transistor M2 is responsive to a signal at the output transistor M3. The signal at the output transistor M3 may be the output voltage V_{out} or the drain to source current I_{M3} of the output transistor M3. The range-limited buffer transistor M2 has two modes, depending on the magnitude of the signal at the output transistor M3. One mode, the "buffer mode," may be associated with the "voltage regulation" operating mode of the circuit 100. In this mode, the range-limited buffer transistor M2 allows the error amplifier 110 to regulate the output voltage V_{out} . A second mode, the "switch mode," may be associated with the "current-limiting" mode of the circuit 100. In the second mode, the range-limited buffer transistor M2 allows a current in the circuit 100 to be mirrored to the output transistor M3, such that the output transistor current I_{M3} is limited. It is noted that limiting the output transistor current I_{M3} may also limit the load current I_{load} . For example, the current I_{M1} of mirror transistor M1 is mirrored to the output transistor M3 in the current-limiting mode. Throughout this description, the term mirroring a current is not confined to mean mirroring the exact magnitude of current, but may include mirroring some fraction or multiple of a current to the output transistor M3. The fraction or multiple may be pre-determined by appropriate selection of transistor sizes.

The range-limited buffer transistor M2 acts as a source follower buffer on the output of the error amplifier 110 in the voltage regulation mode of operation. Thus, the error amplifier 110 regulates the output voltage during the voltage regulation mode of operation via a regulation
5 loop including the error amplifier 110, the range-limited buffer transistor M2, the output transistor M3, and output resistors R1 and R2.

As previously mentioned, the circuit 100 has a current that is mirrored to the output transistor M3 during the current limiting mode.
10 The generation of that current will now be discussed. Current source I1 supplies "I" amperes of current. Thus, the current in range-limited buffer transistor M2 is limited to "I" amps by the current source I1. Current source I2 sinks $N * I$ amperes, where "N" is a greater than one. This allows current source I2 to sink all of the current from the drain D2 of the range-
15 limited buffer transistor M2, along with additional current from the drain D1 of mirror transistor M1. This configuration means that mirror transistor M1 will have a source to drain current of $I * (N - 1)$ amperes, such that the total current through mirror transistor M1 and range-limited buffer transistor M2 equals the current sunk by current source I2.

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The current sources I1 and I2 serve as bias currents. During voltage regulation mode, they bias up range-limited buffer transistor M2 to operate as a source follower. During current limiting mode, they serve to bias

mirror transistor M1 so that its drain D1 is at a pre-determined voltage level. The mirror transistor M1 clamps the voltage at the gate G3 of the output transistor M3 in order to limit the output current I_{M3} , which will be discussed in more detail later. The current sources I1 and I2 may be
5 proportional to absolute temperature (PTAT), although this is not required. The current sources I1 and I2 may be constructed with a similar technique such that they behave with similar characteristics.

The operation of circuit 100 will now be examined under the
10 condition in which the load current I_{load} increases. If the load current I_{load} begins to increase, the output of the error amplifier 110 will drop to maintain voltage regulation at the circuit output V_{out} . For example, if the output voltage V_{out} drops, this forces down the voltage of the positive input of the error amplifier 110, which in turn causes the output of the error
15 amplifier 110 to drop. As the error amplifier's output drops, the voltage of the source S2 of range-limited buffer transistor M2 drops and pulls the gate G3 of the output transistor M3 lower, allowing the output transistor M3 to source more current.

20 Continuing with the discussion of the operation of the circuit 100, the drain D2 of range-limited buffer transistor M2 is clamped at a fixed voltage. For example, it is clamped at the supply voltage V_{dd} minus the source to gate voltage V_{sg1} of mirror transistor M1. If the voltage of the gate G2 of the

range-limited buffer transistor M2 is forced down to a point such that $[V_{ds2} < (V_{gs2} - V_{t2})]$ by the dropping of the output voltage of the error amplifier 110, the range-limited buffer transistor M2 will operate in its triode region. In triode operation, the range-limited buffer transistor M2 will have a low
5 impedance path between its drain and source terminals. This low impedance path acts to connect M1 and M3 into a current mirror configuration. The circuit 100 is designed such that, at a pre-determined output transistor current level I_{M3} , the range-limited buffer transistor M2 will operate in its triode region. Thus, the source S2 of range-limited buffer
10 transistor M2 is pulled to nearly the same voltage as the drain D2 of the range-limited buffer transistor M2.

When the range-limited buffer transistor M2 operates in triode region, mirror transistor M1 and output transistor M3 form a current
15 mirror. Moreover, the error amplifier 110 is effectively prevented from regulating the voltage output V_{out} when range-limited buffer transistor M2 operates in its triode region. Thus, the output voltage V_{out} is allowed to fall, such that the output current I_{M3} is prevented from exceeding a safe limit. Even if the output of the error amplifier 110 is extremely low, it will not
20 affect the output transistor M3, because the drain D1 of the mirror transistor M1 clamps the voltage of the gate G3 of the output transistor M3. For example, the voltage of the gate G3 of the output transistor M3 is clamped to $V_{dd} - V_{sg1}$. The output current I_{M3} is limited according to

mirror transistor M1 is mirrored in the output transistor M3, the factor depending on the relative dimensions of the two transistors M1, M3.

In embodiments of the present invention, the mirror transistor M1
5 and the output transistor M3 are the same type of device. Therefore, they track well with each other. For example, the effects of process and temperature variations are minimized because the mirror transistor M1 and the output transistor M3 are affected in a similar fashion.

10 An aspect of the operation of circuit 100 as the supply voltage Vdd is turned on will now be discussed. In particular, a case in which the load is capacitive will be discussed. Embodiments of the present invention will slowly ramp up the output voltage, when the load is capacitive. In contrast, some conventional voltage regulators exhibit an undesirable sharp spike in
15 current when facing a capacitive load when turning on the supply voltage. In embodiments of the present invention, the output current IM3 is limited by the drain current IM1 in mirror transistor M1.

Figure 2 is a schematic of a circuit 200 for limiting current in a
20 voltage regulator using a cascode transistor M4, according to an embodiment of the present invention. Various circuit elements in circuit 200 are similar to those in circuit 100 and will not be discussed again. Circuit 200 adds a cascode transistor M4 between output resistor R1 and

output transistor M3. This embodiment is used to reduce or eliminate the effect of channel length modulation. To consider the effect of channel length modulation, Figure 1 will be examined for two arbitrary supply voltages of different magnitudes. For both supply voltages, the drain D3 of output transistor M3 will stay down at V_{out} due to the voltage regulation by the error amplifier 110. However, for the larger of the two supply voltages V_{dd} , the drain to source voltage of output transistor M3 will be larger. Thus, M3 will experience channel length modulation. However, mirror transistor M1 will not experience channel length modulation.

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In Figure 2, the bias voltage V_b of the cascode transistor M4 is a predetermined voltage with respect to the supply voltage V_{dd} . The cascode transistor M4 forces the drain to source voltage V_{ds3} of the output transistor M3 to be substantially constant, regardless of the supply voltage V_{dd} . Thus, channel length modulation is reduced or eliminated, in this embodiment of the present invention.

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Figure 3 is a flowchart illustrating steps of a process 300 of limiting current in a voltage regulation circuit, according to embodiment of the present invention. In step 310, a signal is sensed at an output node.

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In step 320, a determination is made as to whether the signal is above or below a pre-determined threshold. The determination may be made by

circuitry as illustrated and discussed in Figures 1 and 2, although the present embodiment is not so limited.

Step 330 is taken if the signal is below the pre-determined threshold.

- 5 In step 330, a voltage of the output node is regulated. Step 340 is taken if the signal is above the pre-determined threshold. In step 340, a current at the output node is limited without regulating the voltage at the output node. For example, a regulation component that regulated the output voltage in step 330 is prevented from regulating the voltage at the output node in step 340.
- 10 Moreover, a device for regulating a current at the output node is allowed to regulate the output current in step 340.

- The limiting of the current in step 340 may include limiting a voltage at a control gate of an output transistor to a predetermined level to limit the
- 15 current at the output node. The limiting of the current in step 340 may also include mirroring a current in a regulation loop to the output node.

- While embodiments of the present invention have been described in terms of p-channel devices, n-channel devices may also be used. Moreover,
- 20 the present invention is not limited to metal oxide field effect devices, for example, bipolar junction devices may also be used. Embodiments of the present invention are compatible with voltage regulators and battery charging systems; however, the present invention is not limited to use in

voltage regulators and/or battery charging applications. Embodiments of the present invention are well suited for use as a low-dropout (LDO) voltage regulator.

5 Therefore, it will be seen that embodiments of the present invention provide current limitation in a voltage regulation circuit. Further, embodiments of the present invention provide a current limit protection circuit that is compatible with and can be fabricated economically with existing semiconductor fabrication techniques.

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 The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.

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